DVV Clarifications
Metrics Level Deviations

<table>
<tr>
<td>3.3.2</td>
<td>
Number of workshops/seminars conducted on Research methodology, Intellectual Property Rights (IPR),entrepreneurship, skill development during the last five years.

3.3.2.1. Total number of workshops/seminars conducted on Research methodology, Intellectual Property Rights (IPR),entrepreneurship, skill development year-wise during the last five years.

HEI Input :
<table>
<tr><th>2020-21</th><th>2019-20</th><th>2018-19</th><th>2017-18</th><th>2016-17</th></tr>
<tr><td>13</td><td>14</td><td>16</td><td>7</td><td>20</td></tr>
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</td>
<td>Provide detailed report for On Mathematical Methods For Machine Learning (MMMML-2021) Electronics On Anything: How Thin Film Electronics Can Instrument The World Network-On-Chip: A Journey From Electronic To Electronic-Photonic To Future Plasmonic Systems Computing With P-Bits: Between A Bit And A Q-Bit 3D Integration: Above And Beyond Moore'S Law Re-Thinking Computing With Neuro-Inspired Learning: Devices, Circuits, And Systems with photograph with date and captions; title of the workshops / seminars conducted signed by comptetent authority the year 2016-17, 2017-18 , 2018-19 and 2019-20, 2020-21."</td>
</tr>
</table>

Supporting Documents:

Detailed report for

i) On Mathematical Methods for Machine Learning (MMML-2021)

ii) Electronics On Anything: How Thin Film Electronics Can Instrument the World

iii) Network-On-Chip: A Journey from Electronic to Electronic-Photonic to Future Plasmonic Systems

iv) Computing With P-Bits: Between a Bit And a q-Bit

v) 3D Integration: Above and Beyond Moore'S Law

vi) Re-Thinking Computing with Neuro-Inspired Learning: Devices, Circuits, And Systems

Celebrating 20 years

Department of Mathematics,
Heritage Institute of Technology
in association with
ORSI, Kolkata Chapter
Organizes

5- Days Online Workshop on

Mathematical Methods for Machine Learning

September 20 - 24, 2021

10AM - 12 Noon
2PM-4PM

Speakers

Dr. Samarjit Kar
Professor
Department of Mathematics
National Institute of Technology
Durgapur

Dr. Sandip Chatterjee
Associate Professor and Head
Department of Mathematics
Heritage Institute of Technology

Dr. Dipankar Chakraborty
Assistant Professor
Department of Mathematics
Heritage Institute of Technology

Dr. Sk. Arif Ahmed
Postdoctoral Researcher
UiT The Arctic University of Norway
TromsØ, Norway

Topics:

- Linear Algebra
- Multivariate Calculus
- Statistics
- Optimization Algorithms

For Registration, email to:

Prof. Moulipriya Sarkar
Email: moulipriya.sarkar@heritageit.edu
Contact:+91-9433415932
(Workshop Coordinator)

Prerequisite:
High-School Mathematics

Heritage Institute of Technology
Department of Mathematics

Report: Workshop on Mathematical Methods for Machine Learning (MMML-2021), organized by the Department of Mathematics, Heritage Institute of Technology, in association with ORSI, Kolkata Chapter, in online mode (Google meet), on September 20-24,2021.

The Department of Mathematics, Heritage Institute of Technology, in association with ORSI, Kolkata Chapter, organized a 5-day workshop on Mathematical Methods for Machine Learning (MMML-2021) on September 20-24, 2021 in online mode (Google meet), in which the mathematical concepts that are at the foundations of the techniques and algorithms used in machine learning were discussed. The number of participants in the workshop was 40, which was kept low in order to facilitate effective interaction during the workshop. The backgrounds and levels of participants were heterogeneous where the levels are ranging from 1st year students to Assistant Professors in various universities to research scholars even in foreign universities and the background varies among Mathematics, Physics, Chemistry, Civil Engineering, Computer Science, Electronics Engineering and Pharmaceutical Engineering.

The inaugural session, held on September 20, 2021, was graced by the presence of Prof. Basab Choudhuri, Principal, HITK, Prof. R. N. Mukherjee, Prof. Debabrata Datta and Prof.Subhashis Majumder. They addressed the gathering and thereby set the stage for the proceedings of the workshop.

The four distinguished speakers of the workshop were:
(i) Prof. Samarjit Kar, Professor, Department of Mathematics, NIT Durgapur and Secretary, ORSI, Kolkata Chapter.
(ii) Dr. Sandip Chatterjee, Associate Professor and Head, Department of Mathematics, Heritage Institute of Technology, Kolkata.
(iii) Dr. Dipankar Chakraborty, Assistant Professor and DC, Department of Mathematics, Heritage Institute of Technology, Kolkata.
(iv) Dr. Sk. Arif Ahmed, Assistant Professor in the School of Computer Science and Engineering, XIM University, Bhubaneswar.

Dr.Souvik Ghosh compèred the proceedings of the workshop.

On September 20, 2021, after the inaugural session, **Prof. Samarjit Kar** delivered a lecture entitled '***A Basic Introduction to Machine Learning and Data Science***', in which the fundamentals of the subject were discussed. In the second session, **Dr. Sandip Chatterjee** delivered a lecture entitled '***Basics of Linear Algebra: Matrix Transformations, Eigenvectors,***

Diagonalisation, Orthogonalisation and Gram-Schmidt Process', in which the algebraic background of the subject was discussed in detail.

The probabilistic features of the subject were discussed by **Dr. Dipankar Chakraborty** in a talk entitled '***Review of Probability Theory and Random Variables***', in the first session on September 21, 2021. In the second session, **Dr. Sandip Chatterjee** continued the discussion of algebra in his lecture entitled ***'Matrix Factorisation: QR factorisation, Solving Linear Least-square Problems using QR factorisation and Singular Value Decomposition(SVD).***

In the first session of September 22, 2021, **Dr. Dipankar Chakraboty** continued the discussion of probability in a lecture whose title was ***'Joint Probability Distribution and Regression'***. The title of **Prof. Samarjit Kar's** talk in the second session was '***Optimization Methods for Machine Learning and Data Science'.***

On September 23, 2021, Dr. **Sk. Arif Ahmed** delivered a lecture entitled '***Machine Learning and Deep Learning using Python'*** in the first session, and Dr. **Dipankar Chakraborty** discussed the statistical aspects of the subject in the talk '***Regression Analysis***' in the second session.

On September 24, 2021, **Dr. Sk. Arif Ahmed** delivered the second part of his lecture on **'Machine learning and deep learning using Python'**. The title of the lecture delivered by **Dr. Sandip Chatterjee** in the second and final session was ***'Convexity and the Gradient Descent Algorithm'***. At the conclusion Dr. Sandip Chatterjee gave the vote of thanks, thus bringing the workshop to an end.

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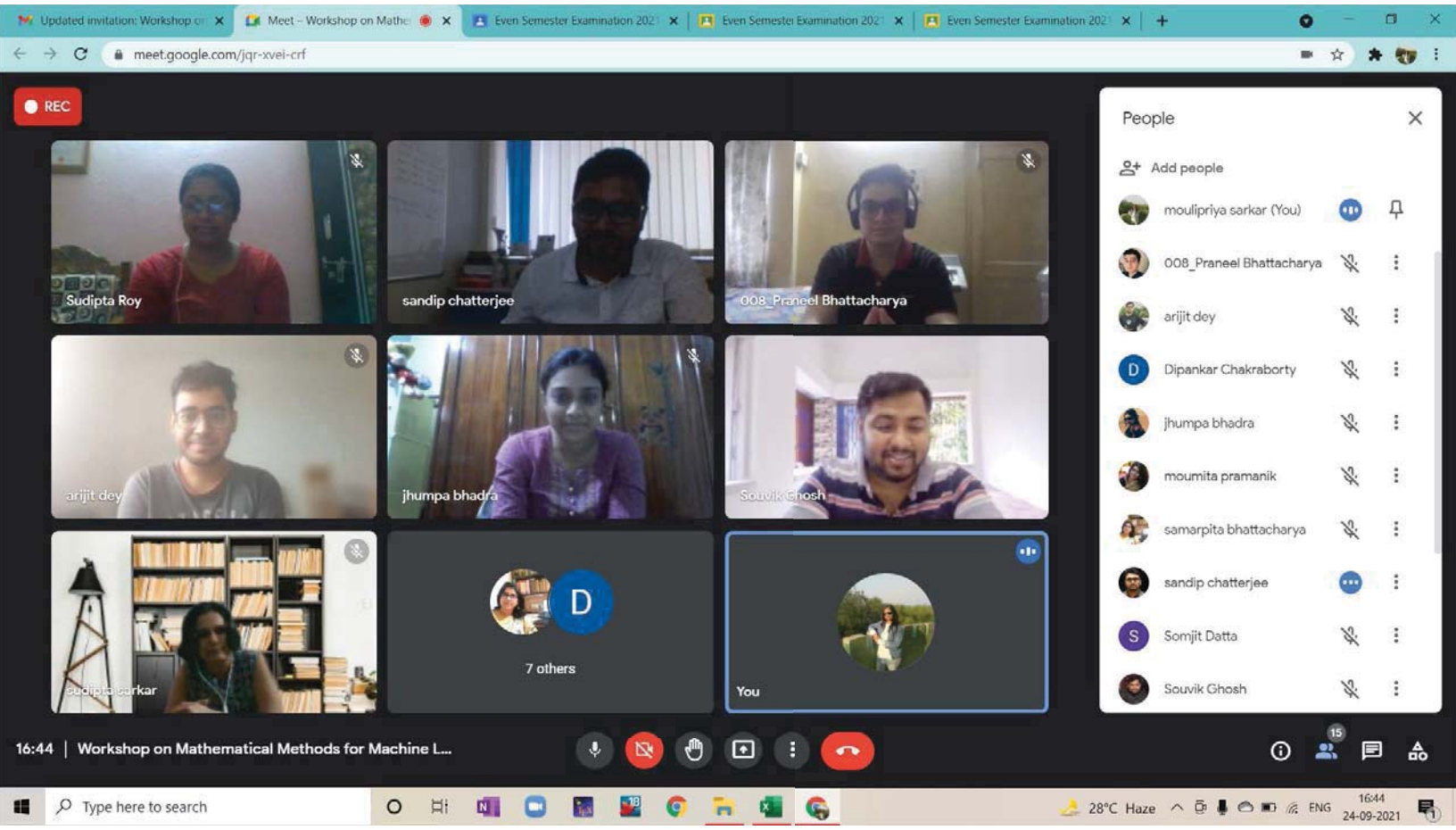
Sandip Chatterjee 14/12/21

(Dr. Sandip Chatterjee)

HOD, Mathematics

Dept. of Mathematics
Heritage Institute of Technology

Workshop On Mathematical Methods For Machine Learning (MMML-2021), September 20 - 24, 2021



Sandip Chatterjee

IEEE EDS DISTINGUISHED LECTURE

Electronics on Anything: How Thin Film Electronics can Instrument the World

Lecture by

Prof. Ioannis (John) Kymissis

Professor of Electrical Engineering, Columbia University, New York, USA

Saturday, 19th June, 2021

7 p.m. (IST)

Free Registration. Limited seats. Register by 18.06.2021 at **https://bit.ly/3wuy3EG**

Organized by: **IEEE EDS Center of Excellence,** Heritage Institute of Technology in association with **IEEE EDS Kolkata Chapter** & **IEEE EDS HITK SBC**

Electronics On Anything: How Thin Film Electronics can Instrument the World

Short abstract:

Silicon electronics have revolutionized the processing and handling of information. The high temperatures required to create crystalline silicon devices, however, has limited the application of crystalline silicon to sensing systems that work in a small and mechanically rigid form factor. The development of inorganic and organic thin film electronics has launched a second revolution in electronics, granting the ability to process electronically active materials at low temperatures. This has allowed for two exciting opportunities: the ability to build electronic devices on large format substrates on the same size scale as the systems they interact with, and the ability to integrate electronic materials on a range of substrates including the back-end of CMOS integrated circuits, electronically active substrates, and flexible materials.

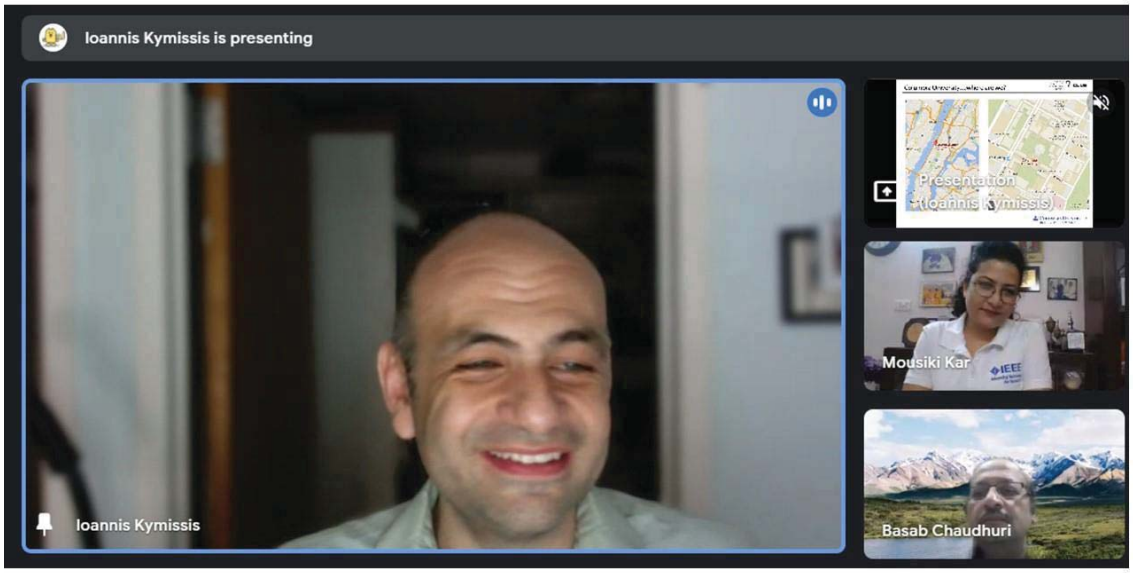
Our group has been working on the hybrid integration of organic semiconductors, thin film piezoelectrics, and laser-recrystallized materials with active substrates to implement a range of new functionalities. In this presentation, I'll show how thin film electronics and the hybrid integration enabled by new semiconductor systems and process options allows for active and spatially localized control of systems that are typically used in a single element format. Devices we have developed include large area and miniature microphones, pressure sensors, active matrix flexible electrostrictive actuators, miniature spectrometers, and active matrix micro-LED displays. These approaches unlock new applications in healthcare, sensing, displays, soft and highly instrumented robotics, transportation, and communications.

Biography:

Ioannis (John) Kymissis graduated with his SB, M.Eng., and Ph.D. degrees from MIT. His M.Eng. thesis was performed as a co-op at the IBM TJ Watson Research Lab on organic thin film transistors, and his Ph.D. was obtained in the Microsystems Technology Lab at MIT working on field emission displays. After graduation he spent three years as a post-doc in MIT's Laboratory for Organic Optics and Electronics working on a variety of organic electronic devices and as a consulting engineer for QDVision.

He joined the faculty at Columbia University in Electrical Engineering in 2006 as an assistant professor. John has won a number of awards for his work, including the NSF CAREER award, the IEEE EDS Paul Rappaport award, the Vodaphone Americas Foundation Wireless Innovation Award, the MIT Clean Energy Prize, and a Verizon Powerful Answers award. He recently served a term as the editor in chief of the Journal of the Society for Information Display, is a fellow of the SID, and was the general chair for the 2014 Device Research Conference.

The Month of June was graced by a Distinguished lecture by Prof. Ioannis (John) Kymissis , Professor of Electrical Engineering in the Department of Electrical Engineering at Columbia University, New York, USA. He spoke on the topic 'Electronics on Anything: How Thin Film Electronics can Instrument the World' on June 19, 2021 at 7 p.m. IST.



DL Prof. Ioannis (John) Kymissisdelivering his lecture

In his lecture Prof. Kymissis discussed how his group has been working on the hybrid integration of organic semiconductors, thin film piezoelectrics, and laser-recrystallized materials with active substrates to implement a range of new functionalities. Devices they have developed include large area and miniature microphones, pressure sensors, active matrix flexible electrostrictive actuators, miniature spectrometers, and activematrix micro-LED displays. These approaches unlock new applications in healthcare, sensing, displays, soft and highly instrumented robotics, transportation, and communications.

The lecture was enjoyed by 50 attendees. The event was organizedin association with IEEE EDS Kolkata Chapter.

HOD, ECE Department
Heritage Institute of Technology
Kolkata

Network-on-Chip : A Journey from Electronic to Electronic-Photonic to Future Plasmonic Systems

Lecture by

Prof. Prasanta Kumar Basu

Ex-Professor, Institute of Radio Physics and Electronics, University of Calcutta.

Saturday, 5th June, 2021

7 p.m. (IST)

Free Registration. Limited seats. Register by 03.06.2021 at t.ly/Yoed

Organized by: **IEEE EDS Center of Excellence,** Heritage Institute of Technology in association with **IEEE EDS Kolkata Chapter**

NETWORK-ON-CHIP : A JOURNEY FROM ELECTRONIC TO ELECTRONIC-PHOTONIC TO FUTURE PLASMONIC SYSTEMS

P K Basu
Retired professor, Institute of Radio Physics and Electronics, University of Calcutta
92 Acharya Prafulla Chandra Road, Kolkata 700009
e-mail: pkbasu.rpe@ieee.org//pkbasu.cal @gmail.com

ABSTRACT

Miniaturization of electronic circuits began with the advent of transistors and continued with galloping pace after the first proposal of IC and subsequent development of planar technology. Introduction of MOS and then CMOS and subsequent scaling laws revolutionalized chip development following Moore's law. With ingenious technology to combat short channel effects, individual transistors having feature lengths in sub-5 nm regime have been announced. The remarkable development notwithstanding, the network-on-chip (NOC) involving complex circuits faces the problem of high power dissipation due to interconnect bottleneck, degrading the performance of data centres and high performance computers.

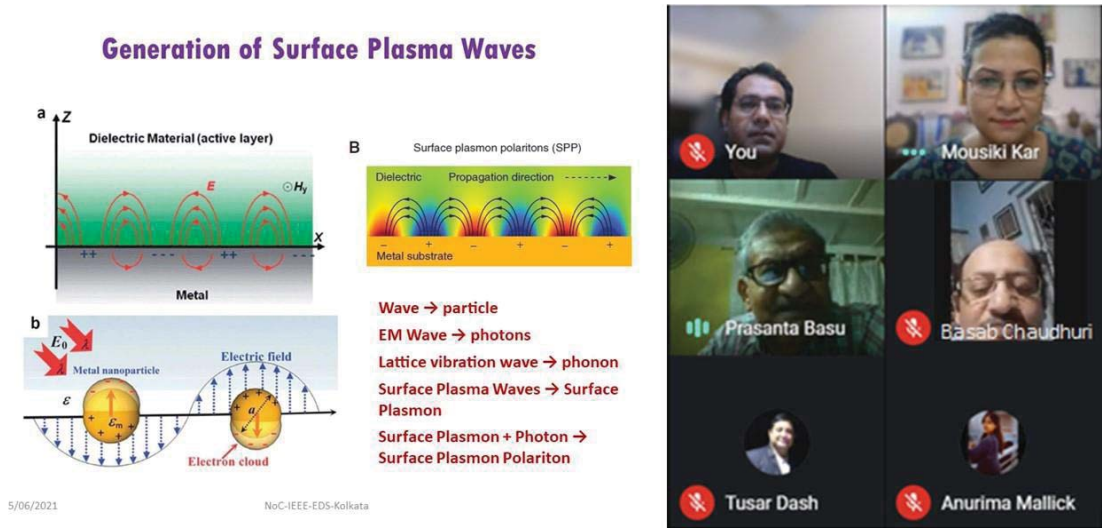
Photonics, particularly on silicon platform, are thought to offer viable solution to the interconnect problem and electronic-photonic integration on Si is currently a hot topic for R&D activities. The poor emission from Si requires hybrid integration with III-V compound and alloy based lasers and encourages intensive research on GeSn alloys for lasers and other photonic components.

The ultimate size of photonic devices is however diffraction limited, which allows individual devices to have size of light wavelength in the micrometer range. Plasmonics, in particular surface plasmonics, allow realization of sub wavelength sized devices and therefore seems to be the ultimate solutions for NOC. The very small propagation length of plasmonic waves can be overcome by Surface Plasmon Amplification by Stimulated Emission of Radiation (SPASER) replacing nanolasers used in communication and networking. The area is still in its infancy, but is subject of current intense research. The proposed webinar aims to cover the important milestones and to present current state-of the-art technology.

Prasanta Kumar Basu, B.Sc. (Physics, Presidency), B.Tech, M.Tech, Ph.D. all from RPE-CU joined RPE Department as a Lecturer in 1971, retired from CU in 2011 and then worked as UGC BSR Faculty Fellow, Visiting Professors at IIT KGP and National Chung Cheng University, Taiwan, and as Investigator in an Indo-Taiwan project. In his long career as teacher, researcher, and administrator, he had more than 130 papers, many conference papers, 4 books and 2 book chapters, and he guided 20 odd Ph.D. students. He initiated an international conference series *CODEC* and earned for the department the title *UGC Networking Resource Centre in Physical Sciences*: the first in India. He worked as a post doc in Belgium, Alexander von Humboldt fellow in Germany, first INSA Research fellow, visiting professors in TIFR, and McMaster University, Canada, INSA-Royal Society Exchange professor in

UK. He also served for 8 years as a member of EPSRC College, UK, to review their projects. Currently, he is engaged in joint research and book writing with faculties of RPE, NIT Delhi, McMaster University and National CC Univ- Taiwan.

Following this a lecture was delivered by Prof. Prasanta Kumar Basu, Ex-Professor, Institute of Radio Physics and Electronics, University of Calcutta on June 05, 2021 at 7 p.m. IST. The topic of the webinar was 'Network-on-Chip: A Journey from Electronic to Electronic-Photonic to Future Plasmonic Systems'.



Prof. Prasanta Kumar Basu delivering his lecture

Prof. Prasanta Kumar Basu, discussed how plasmonics, in particular surface plasmonics, allow realization of sub wavelength sized devices and therefore seems to be the ultimate solutions for network-on-chip (NOC). The very small propagation length of plasmonic waves can be overcome by Surface Plasmon Amplification by Stimulated Emission of Radiation (SPASER) replacing nanolasers used in communication and networking. Th talk was attended by 97 participants.

HOD, ECE Department
Heritage Institute of Technology
Kolkata

EDS DISTINGUISHED LECTURE

COMPUTING WITH P-BITS: BETWEEN A BIT AND A Q-BIT

By Prof. Supriyo Datta, *Purdue University*

DATE: SATURDAY, MAY 29, 2021

TIME: 7:30 PM IST

Please register at https://bit.ly/3f6evAa by May 27, 2021

Organized by: IEEE Kolkata Section, IEEE EDS Heritage Institute of Technology SBC

IEEE EDS Center of Excellence, Heritage Institute of Technology, Kolkata

IEEE KOLKATA SECTION

ELECTRON DEVICES SOCIETY

Abstract: Computing with p-Bits: Between a Bit and a q-Bit

Digital computing is based on a deterministic bit with two values, 0 and 1. On the other hand, quantum computing is based on a q-bit which is a delicate superposition of 0 and 1. This talk draws attention to something in-between namely, a p-bit which is a robust classical entity fluctuating between 0 and 1.

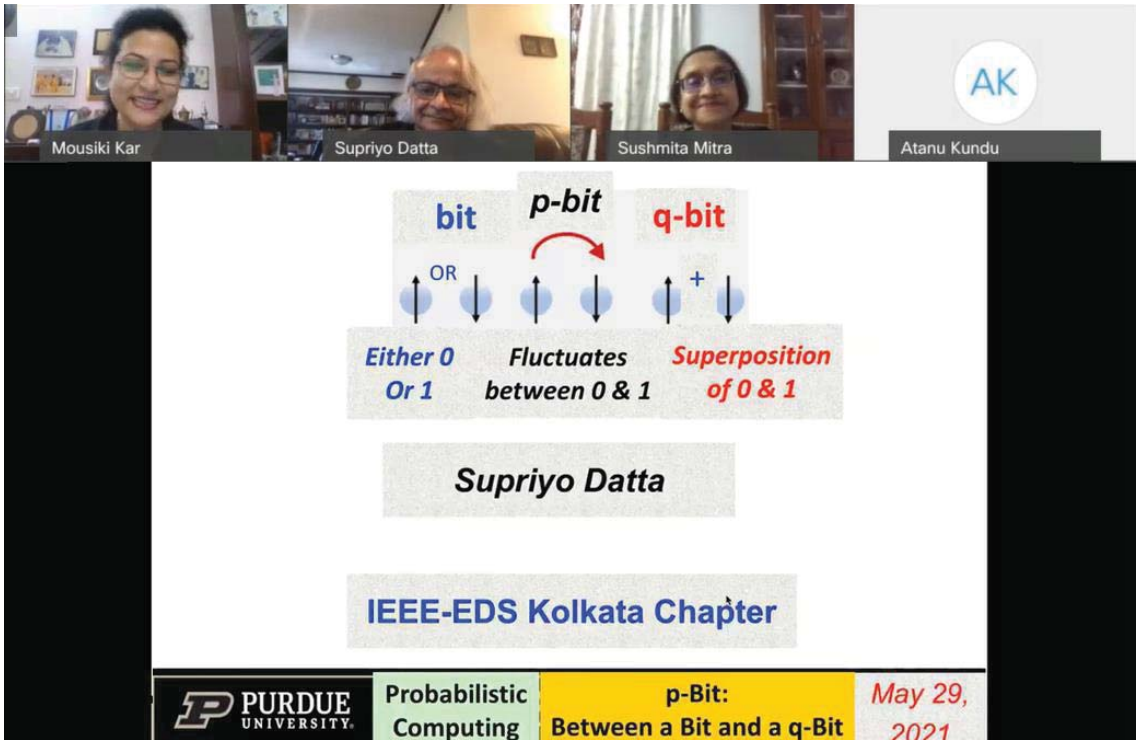
Feynman [1] used the concept of a probabilistic computer as a counterpoint to the quantum computer, noting that "the only difference between a probabilistic classical world and the equations of the quantum world is that the probabilities would have to go negative" The awesome power of quantum computing comes from exploiting these negative (more generally complex) probabilities, which in turn requires stringent experimental conditions to protect the phase.

A probabilistic computer by contrast can be built with existing technology to operate at room temperature as we have demonstrated experimentally [2]. They lack the magic of complex probabilities, but can address a wide variety of problems ranging from optimization and sampling to quantum computing and machine learning [3].

[1] R.P. Feynman, *Int. J. Theor. Phys.* **21**, 467 (1982).
[2] W.A. Borders et al. *Nature* **573**, 390 (2019).
[3] B.M. Sutton et al. *IEEE Access* **8**, 157238 (2020).

Biography: Prof. Supriyo Datta received his PhD from University of Illinois at Urbana-Champaign in 1979 working on surface acoustic wave devices, and has been with Purdue University since 1981. The non-equilibrium Green function (NEGF) method approach pioneered by his group for the description of quantum transport has been widely adopted in the field of nanoelectronics. He is also known for innovative theoretical proposals that have inspired new fields of research including molecular thermoelectricity, negative capacitance devices, and spintronics.

We wound up the month of May with a Distinguished lecture delivered by Prof. Supriyo Datta from Purdue University on the topic ‘Computing with p-Bits: Between a Bit and a q-Bit’onMay 29, Saturday, 7.30 pm (IST).



DL Prof. Supriyo Datta, being greeted by Dr. Susmita Mitra, Chair, Kolkata Section and Dr. Mousiki Kar, Co-ordinator IEEE EDS CoE, HITK and Chair, EDS Kolkata Chapter

He discussed that the awesome power of quantum computing comes from exploiting negative probabilities, which in turn requires stringent experimental conditions to protect the phase. Prof. Supriyo Datta explained that a probabilistic computer by contrast can be built with existing technology to operate at room temperature and has been demonstrated experimentally.

179 participants attended the talk which was organizedin association with IEEE Kolkata Section, IEEE EDS Kolkata Chapterand ED Heritage Institute of Technology Student Branch Chapter.

HOD, ECE Department
Heritage Institute of Technology
Kolkata

IEEE EDS DISTINGUISHED LECTURE

3D Integration: Above & Beyond Moore's Law

Lecture by

Prof. Jesús A. del Alamo

Professor of Electrical Engineering,

Massachusetts Institute of Technology.

Saturday, 8th May, 2021

7 p.m. (IST)

Free Registration. Register by 06.05.2021 at t.ly/PVDb

Organized by: **IEEE EDS Center of Excellence,** Heritage Institute of Technology in association with **IEEE EDS Kolkata Chapter** & **IEEE EDS HITK SBC**

Jesús A. del Alamo

MTL microsystems technology laboratories

- Home
- Team
- Research
- Teaching
- (New!) Integrated Microelectronic Devices
- Brief Bio
- Publications
- In the News
- Image Gallery
- Contact

Jesus giving a talk at the 2004 Microsoft Research Faculty Summit.

Brief Bio

Jesús del Alamo is Director of the Microsystems Technology Laboratories, Donner Professor, and Professor of Electrical Engineering in the Department of Electrical Engineering and Computer Science at MIT.

He holds degrees from Polytechnic University of Madrid (Telecommunications Engineer, 1980), and Stanford University (MS EE, 1983 and PhD EE, 1985). From 1977 to 1981 he was with the Institute of Solar Energy of the Polytechnic University of Madrid, investigating silicon photovoltaics. From 1981 to 1985, he carried out his PhD dissertation at Stanford University on minority carrier transport in heavily doped silicon. From 1985 to 1988 he was research engineer with NTT LSI Laboratories in Atsugi (Japan) where he conducted research on III-V heterostructure field-effect transistors. He joined MIT in 1988.

Over the years, Prof. del Alamo has carried out research on transistors and other electronic devices in a variety of material systems. He has worked on Si solar cells, Si Bipolar Junction Transistors, Si Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), SiGe heterostructure devices, GaAs Pseudomorphic High Electron Mobility Transistors (PHEMTs), InGaAs High Electron Mobility Transistors (HEMTs) and MOSFETs, InGaSb HEMTs, GaN HEMTs and MOSFETs, and more recently Diamond MOSFETs. He has also investigated quantum-effect devices based on AlGaAs/GaAs heterostructures. His current research interests focus on the physics, technology, modeling and reliability of new III-V compound semiconductor field-effect transistors for future logic applications. He is also interested in fundamental reliability physics of GaN transistors for RF power amplification and power switching applications. In addition, Prof. del Alamo is investigating the technology and pedagogy of online laboratories for science and engineering education (the iLab Project).

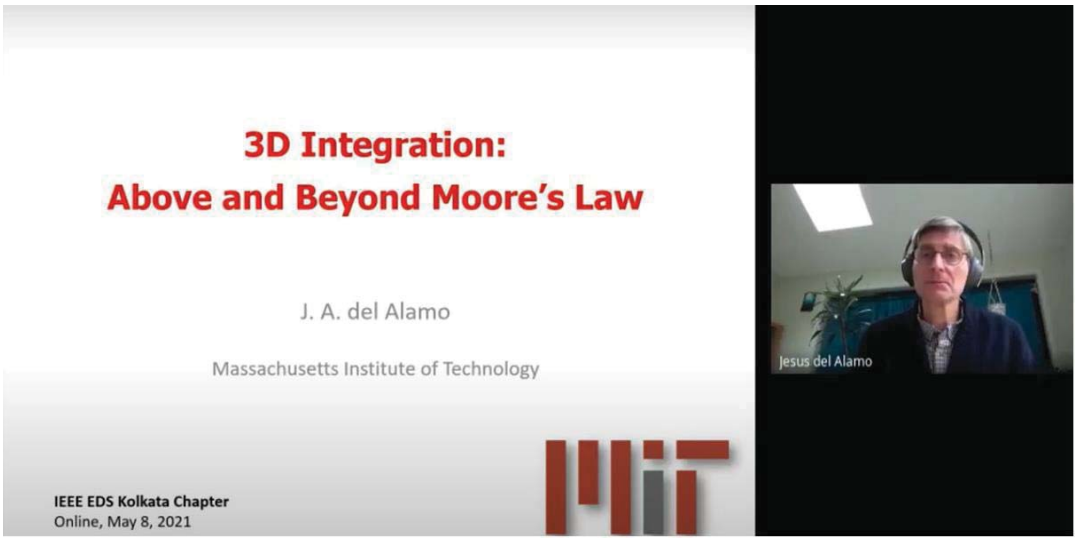
Prof. del Alamo's students have earned numerous best paper awards at national and international conferences. For his research on InGaAs Quantum-Well Field-Effect Transistors he was awarded the 2012 Intel Outstanding Researcher Award in Emerging Research Devices and the Semiconductor Research Corporation 2012 Technical Excellence Award.

Prof. del Alamo teaches undergraduate and graduate-level courses in electronics, electron devices and circuits, and advanced semiconductor device physics. Prof. del Alamo has received several teaching and achievement awards at MIT. In 1992 he was awarded the Baker Memorial Award for Excellence in Undergraduate Teaching. In 1993 he received the H. E. Edgerton Junior Faculty Achievement Award. In 2001, he received the Louis D. Smullin Award for Excellence in Teaching. In 2002, he received the Amar Bose Award for Excellence in Teaching. In 2003, he was named a MacVicar Faculty Fellow. In 2007, Prof. del Alamo was appointed Donner Professor. In 2012, Prof. del Alamo was awarded the IEEE 2012 Electron Devices Society Education Award "For pioneering contributions to the development of online laboratories for microelectronics education on a worldwide scale."

From 1991 to 1996, Prof. del Alamo was an National Science Foundation Presidential Young Investigator. In 1999 he was elected a corresponding member of the Royal Spanish Academy of Engineering. In 2005, he was elected a Fellow of the IEEE and in 2014 he was elected a Fellow of the American Physical Society.

Among other activities, Prof. del Alamo was Editor of IEEE Electron Device Letters from 2005 to 2014 and since 2013 he is the Director of the Microsystems Technology Laboratories at MIT.

The second lecture in the month of May was delivered byProf. Jesús A. del Alamo, Professor at Massachusetts Institute of Technology (MIT) and Director of the Microsystems Technology Laboratories. Prof. Alamo, spoke on the topic '3D Integration: Above and Beyond Moore's Law' on May 08, 2021, Saturday, at 7 p.m. IST.

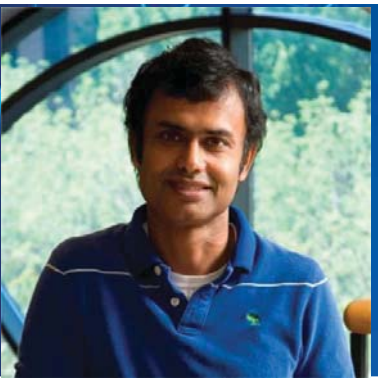


DL Prof. Jesús A. del Alamo delivering his lecture

Three-dimensional (3D) integration which is an emerging technology that can form highly integrated systems by vertically stacking and connecting various materials, technologies and functional components together was discussed. The potential benefits of 3D integration can vary depending on approach; they include multifunctionality, increased performance, reduced power, small form factor, reduced packaging, increased yield and reliability, flexible heterogeneous integration and reduced overall costs.

80 attendees from across the country enjoyed his lucid and informative presentation. The event was organized in association with, IEEE EDS Kolkata Chapter.

HOD, ECE Department
Heritage Institute of Technology
Kolkata



IEEE DISTINGUISHED LECTURE

Organized by:

IEEE Kolkata Section

IEEE EDS Heritage Institute of Technology SBC

IEEE EDS CENTER OF EXCELLENCE, HITK

Re-Thinking Computing with Neuro-Inspired Learning: Devices, Circuits, and Systems

By Prof. Kaushik Roy

Purdue University, West Lafayette

DATE: SATURDAY, MAY 01, 2021 TIME: 7.30 PM IST

Please register at https://bit.ly/3nfgjcA by April 29, 2021

IEEE KOLKATA SECTION

HERITAGE INSTITUTE OF TECHNOLOGY आत्म दीपो भव KOLKATA

ELECTRON DEVICES SOCIETY®

Abstract of the talk: Re-Thinking Computing with Neuro-Inspired Learning: Devices, Circuits, and Systems

Advances in machine learning, notably deep learning, have led to computers matching or surpassing human performance in several cognitive tasks including vision, speech and natural language processing. However, implementation of such neural algorithms in conventional "von-Neumann" architectures are several orders of magnitude more area and power expensive than the biological brain. Hence, we need fundamentally new approaches to sustain exponential growth in performance at high energy-efficiency beyond the end of the CMOS roadmap in the era of 'data deluge' and emergent data-centric applications. Exploring the new paradigm of computing necessitates a multi-disciplinary approach: exploration of new learning algorithms inspired from neuroscientific principles, developing network architectures best suited for such algorithms, new hardware techniques to achieve orders of improvement in energy consumption, and nanoscale devices that can closely mimic the neuronal and synaptic operations of the brain leading to a better match between the hardware substrate and the model of computation. In this talk, I will focus on our recent works on neuromorphic computing with spike based learning and the design of underlying hardware that can lead to quantum improvements in energy efficiency with good accuracy.

Biography of Prof. Kaushik Roy

Kaushik Roy received B.Tech. degree in electronics and electrical communications engineering from the Indian Institute of Technology, Kharagpur, India, and Ph.D. degree from the electrical and computer engineering department of the University of Illinois at Urbana-Champaign in 1990. He was with the Semiconductor Process and Design Center of Texas Instruments, Dallas, where he worked on FPGA architecture development and low-power circuit design. He joined the electrical and computer engineering faculty at Purdue University, West Lafayette, IN, in 1993, where he is currently Edward G. Tiedemann Jr. Distinguished Professor. He also the director of the center for brain-inspired computing (C-BRIC) funded by SRC/DARPA. His research interests include neuromorphic and emerging computing models, neuro-mimetic devices, spintronics, device-circuit-algorithm co-design for nano-scale Silicon and non-Silicon technologies, and low-power electronics. Dr. Roy has published more than 800 papers in refereed journals and conferences, holds 28 patents, supervised 91 PhD dissertations, and is co-author of two books on Low Power CMOS VLSI Design (John Wiley & McGraw Hill).

Dr. Roy received the National Science Foundation Career Development Award in 1995, IBM faculty partnership award, ATT/Lucent Foundation award, 2005 SRC Technical Excellence Award, SRC Inventors Award, Purdue College of Engineering Research Excellence Award, Outstanding Mentor Award in 2021, Humboldt Research Award in 2010, 2010 IEEE Circuits and Systems Society Technical Achievement Award (Charles Desoer Award), IEEE TCVLSI Distinguished Research Award in 2021, Distinguished Alumnus Award from Indian Institute of Technology (IIT), Kharagpur, Fulbright-Nehru Distinguished Chair, DoD Vannevar Bush Faculty Fellow (2014-2019), Semiconductor Research Corporation Aristotle award in 2015, and best paper awards at 1997

International Test Conference, IEEE 2000 International Symposium on Quality of IC Design, 2003 IEEE Latin American Test Workshop, 2003 IEEE Nano, 2004 IEEE International Conference on Computer Design, 2006 IEEE/ACM International Symposium on Low Power Electronics & Design, 2005 and 2019 IEEE Circuits and system society Outstanding Young Author Award (Chris Kim, Abhronil Sengupta), 2006 IEEE Transactions on VLSI Systems best paper award, 2012 ACM/IEEE International Symposium on Low Power Electronics and Design best paper award, 2013 IEEE Transactions on VLSI Best paper award. Dr. Roy was a Purdue University Faculty Scholar (1998-2003). He was a Research Visionary Board Member of Motorola Labs (2002) and held the M. Gandhi Distinguished Visiting faculty at Indian Institute of Technology (Bombay) and Global Foundries visiting Chair at National University of Singapore. He has been in the editorial board of IEEE Design and Test, IEEE Transactions on Circuits and Systems, IEEE Transactions on VLSI Systems, and IEEE Transactions on Electron Devices. He was Guest Editor for Special Issue on Low-Power VLSI in the IEEE Design and Test (1994) and IEEE Transactions on VLSI Systems (June 2000), IEE Proceedings -- Computers and Digital Techniques (July 2002), and IEEE Journal on Emerging and Selected Topics in Circuits and Systems (2011). Dr. Roy is a fellow of IEEE.

The month of May started off with a lecture delivered by Prof. Kaushik Roy from Purdue University on May 01, Saturday, 7.30 pm (IST). He spoke on the topic, 'Re-Thinking Computing with Neuro-Inspired Learning: Devices, Circuits, and Systems'.

DL Prof. Kaushik Roy, being greeted by Dr. Susmita Mitra, Chair, Kolkata Section, Dr. Atanu Kundu, Chapter Advisor ED HITK SBC and Dr. Mousiki Kar, Co-ordinator IEEE EDS CoE, HITK and Chair, EDS Kolkata Chapter

He described his recent work on neuromorphic computing with spike based learning and the design of underlying hardware that can lead to quantum improvements in energy efficiency with good accuracy. The lecture was attended by 95 participants. The event was organized in association with, ED Heritage Institute of Technology Student Branch Chapter and IEEE Kolkata Section.

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Kolkata